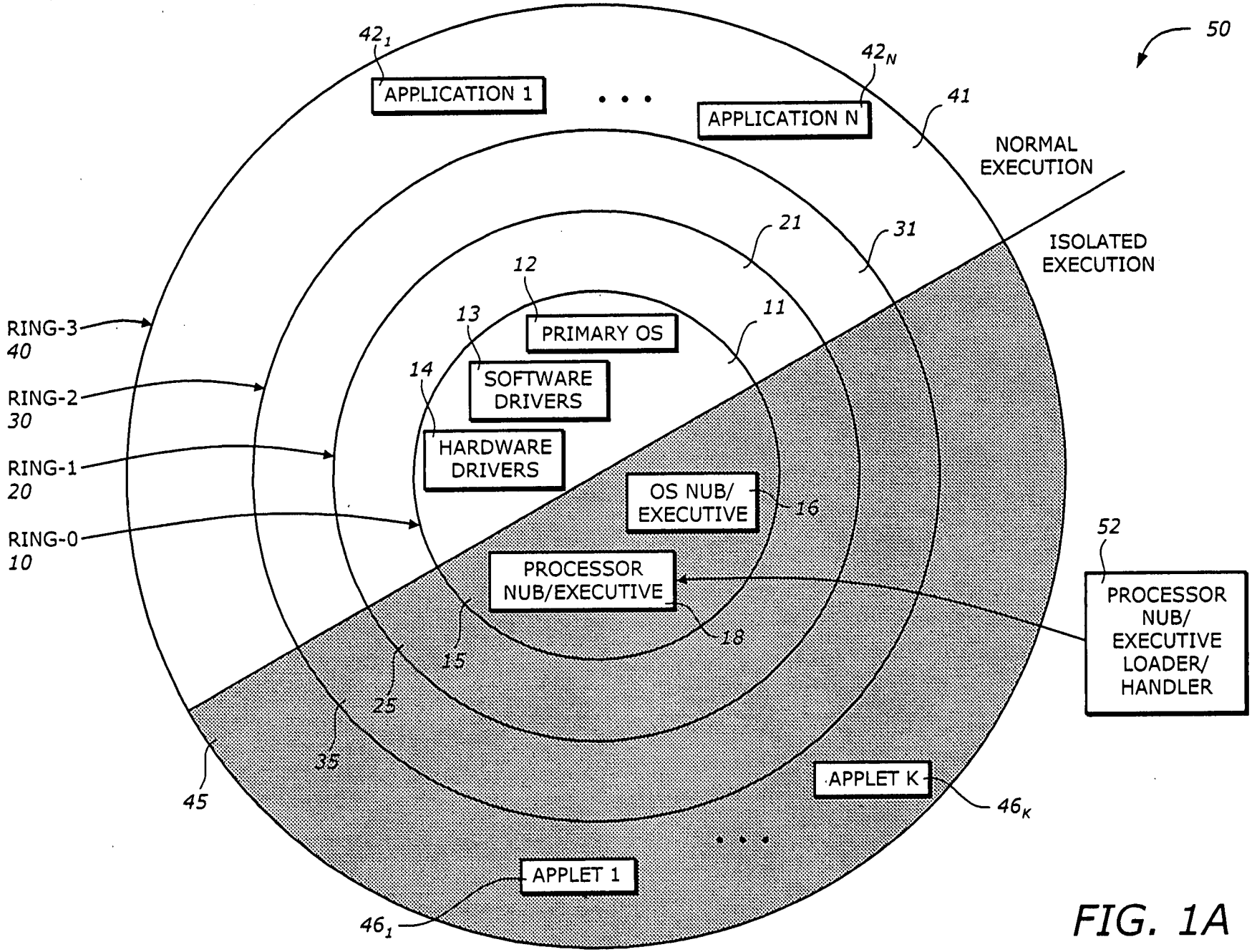
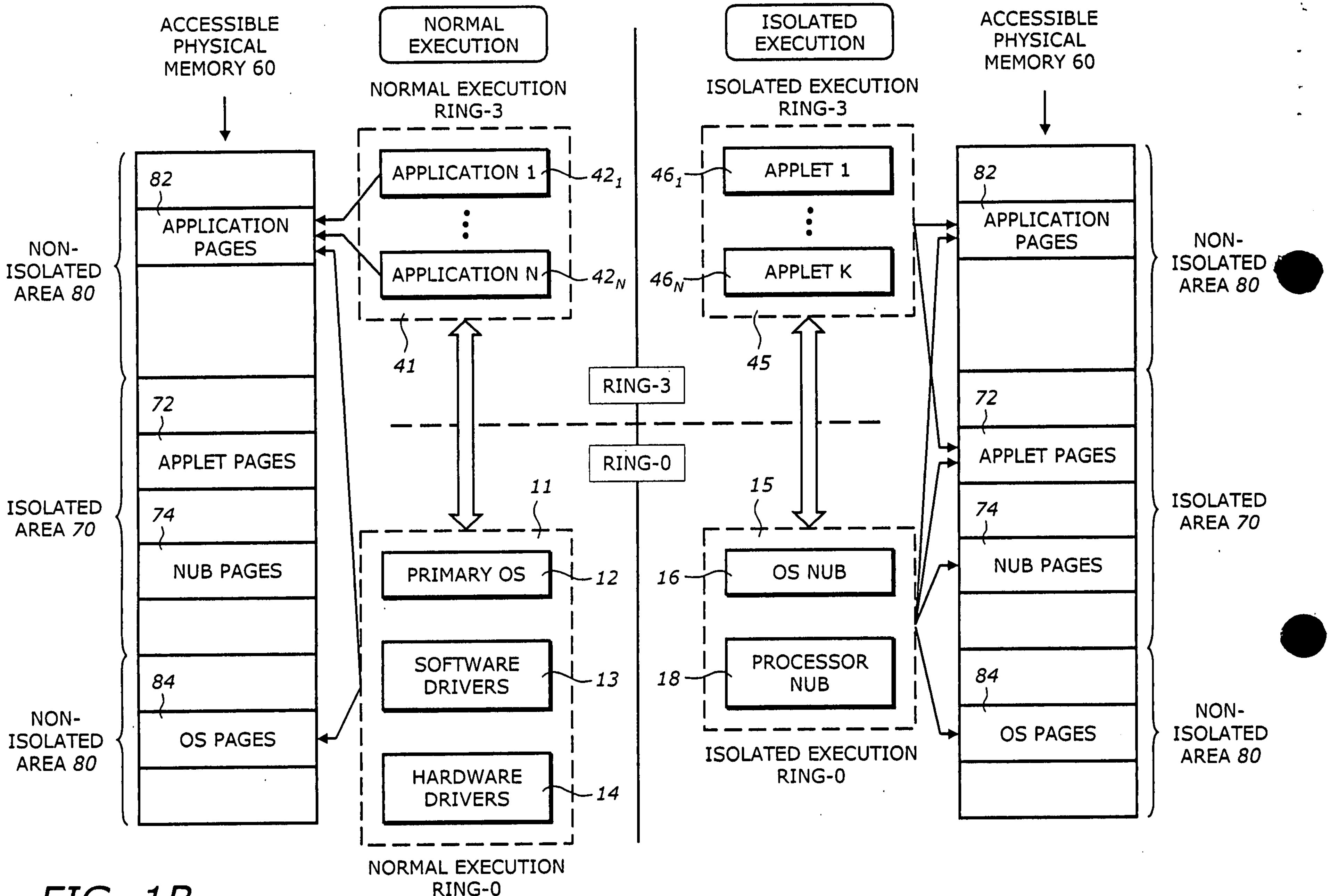


FIG. 1A


ACCESSIBLE PHYSICAL MEMORY 60
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NORMAL EXECUTION RING-3
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ISOLATED EXECUTION RING-3
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16
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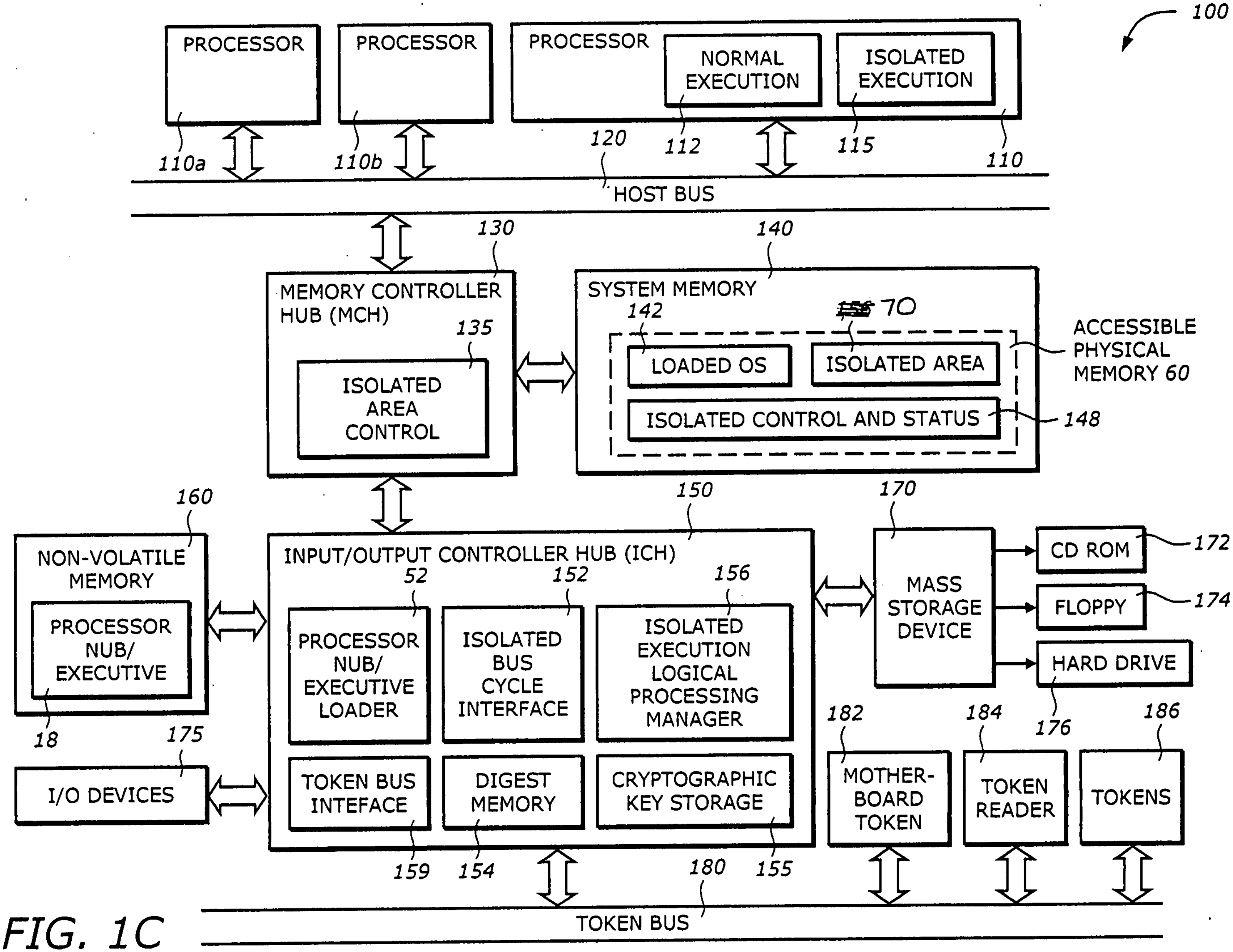
18
PROCESSOR NUB
84
OS PAGES
NORMAL EXECUTION RING-0
ISOLATED EXECUTION RING-0

FIG. 1B



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110a
PROCESSOR
110b
PROCESSOR
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112
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130
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ISOLATED EXECUTION LOGICAL PROCESSING MANAGER
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174
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FIG. 1C

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00TEE0"4S68ES60

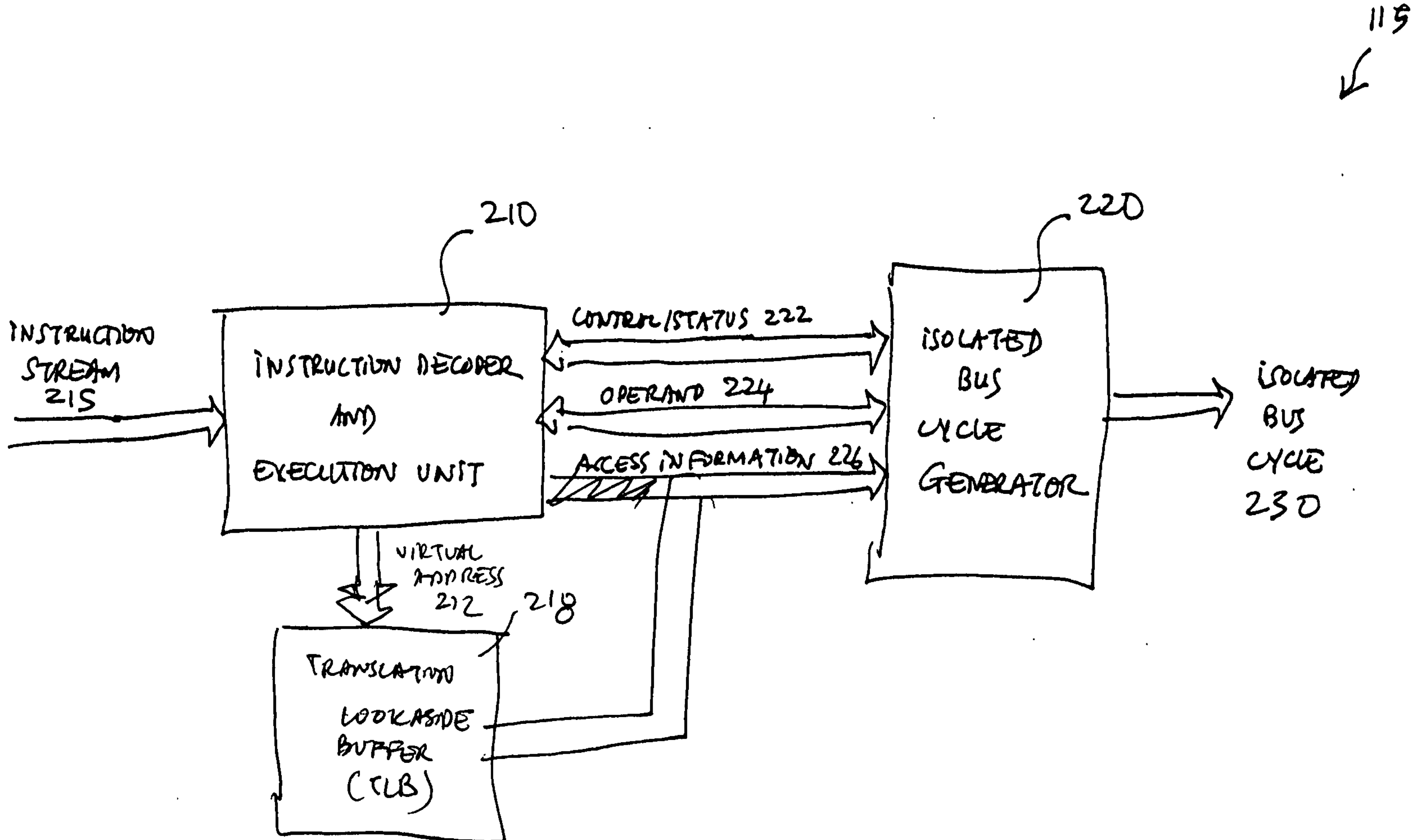

FIG. 2A

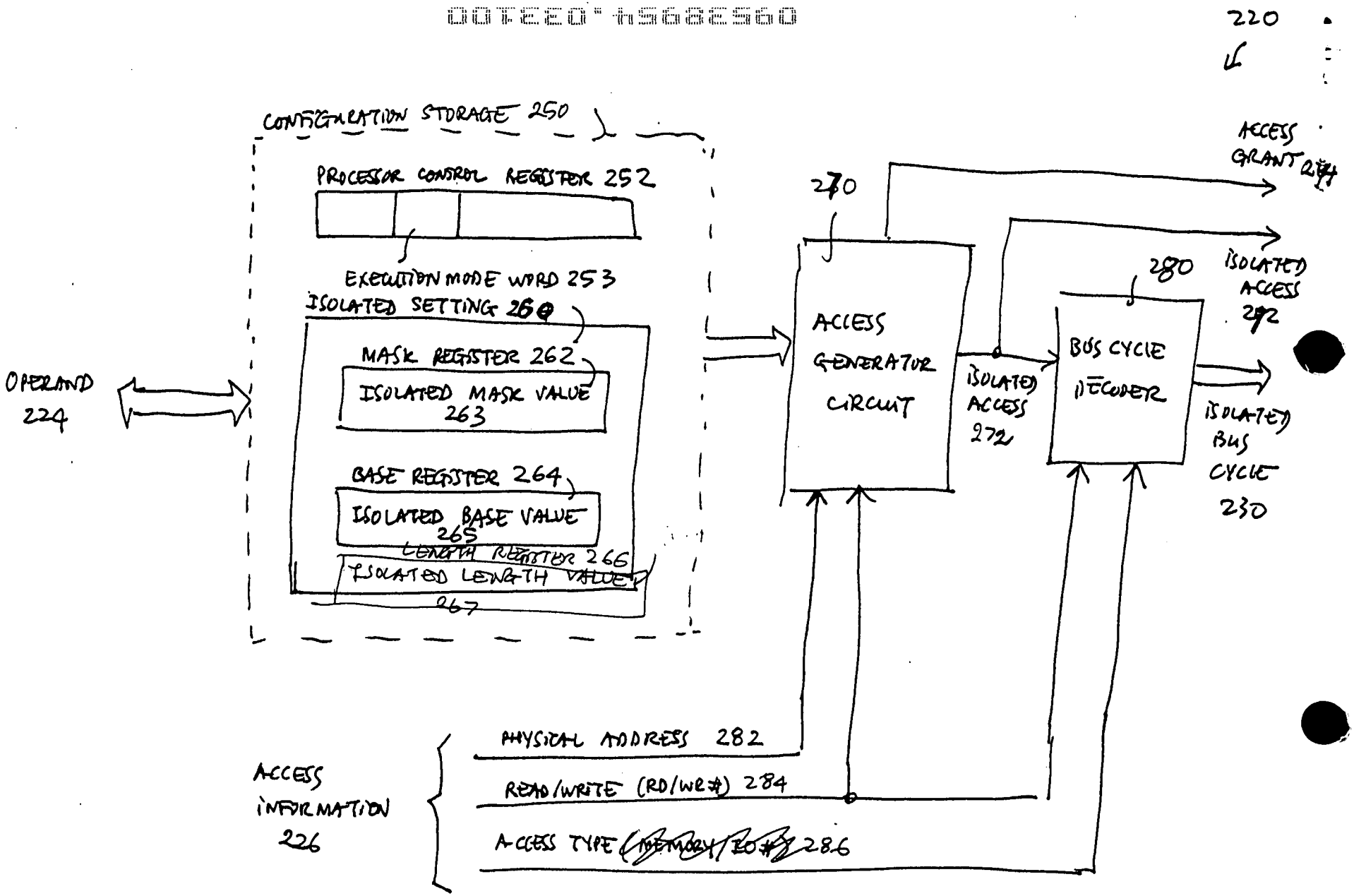
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FIG. 2B

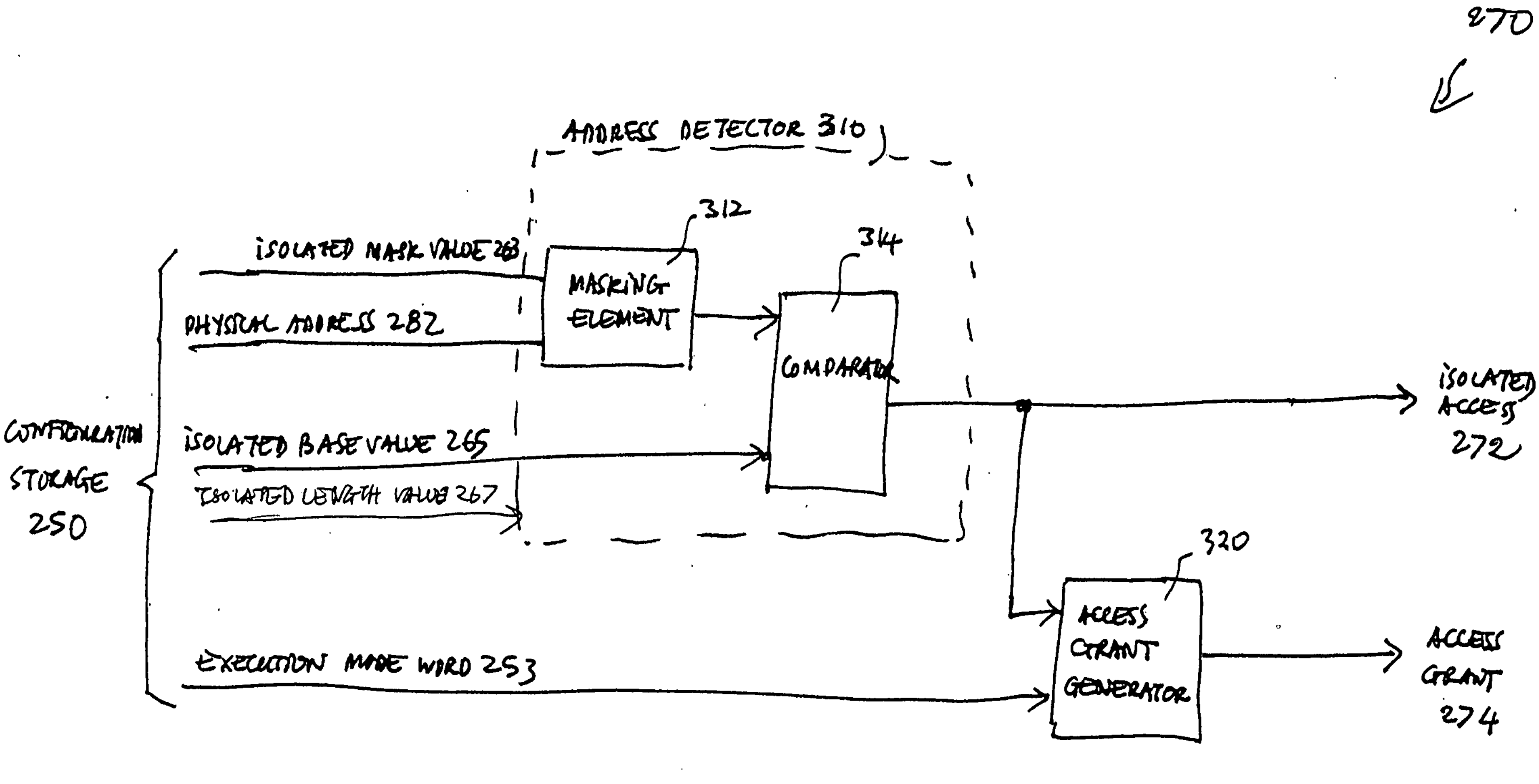
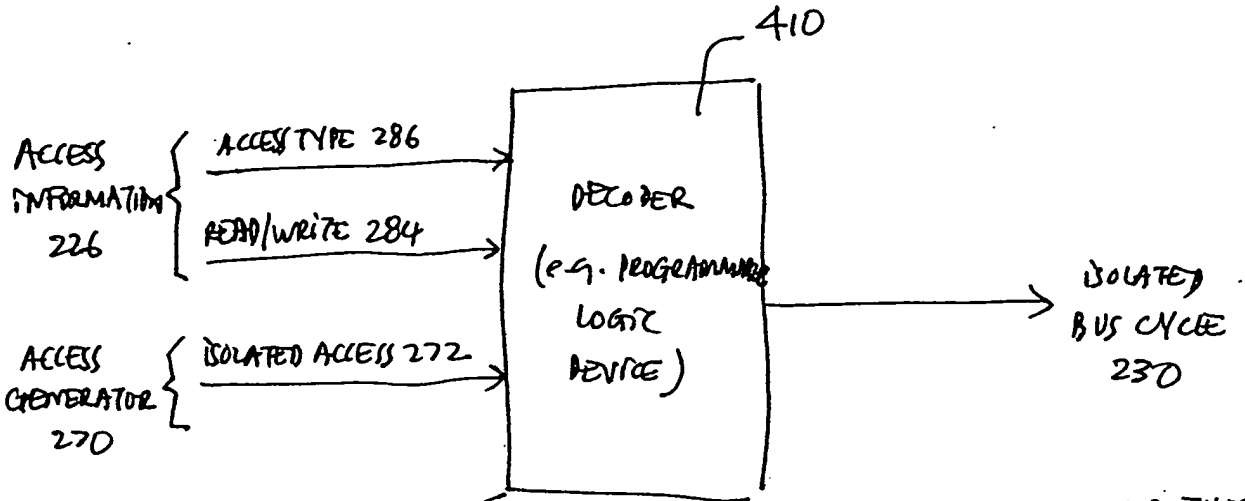


FIG. 3



TRUTH TABLE 420

ACCESS TYPE			ISOLATED ACCESS	ISOLATED BUS CYCLE		RING LEVEL
ISOLATED ENABLED STATE	M/IO#	RD/WR#				
X	X	X	DE-ASSERTED	NOT AVAILABLE		0
ENTRY (e.g., ISO_INIT)	X	X	ASSERTED	THREAT ENTRY	THREAT CYCLE	0
WITHDRAW (e.g., ISO_CLOSE)	X	X	ASSERTED	THREAT WITHDRAWAL		0
X	MEMORY REFERENCE	READ	ASSERTED	ISOLATED DATA READ	DATA ACCESS CYCLE	0
X	MEMORY REFERENCE	WRITE	ASSERTED	ISOLATED DATA WRITE		0
X	I/O REFERENCE	READ	ASSERTED	ISOLATED CONTROL READ	CONTROL ACCESS CYCLE	0
X	I/O REFERENCE	WRITE	ASSERTED	ISOLATED CONTROL WRITE		0

FIG. 4

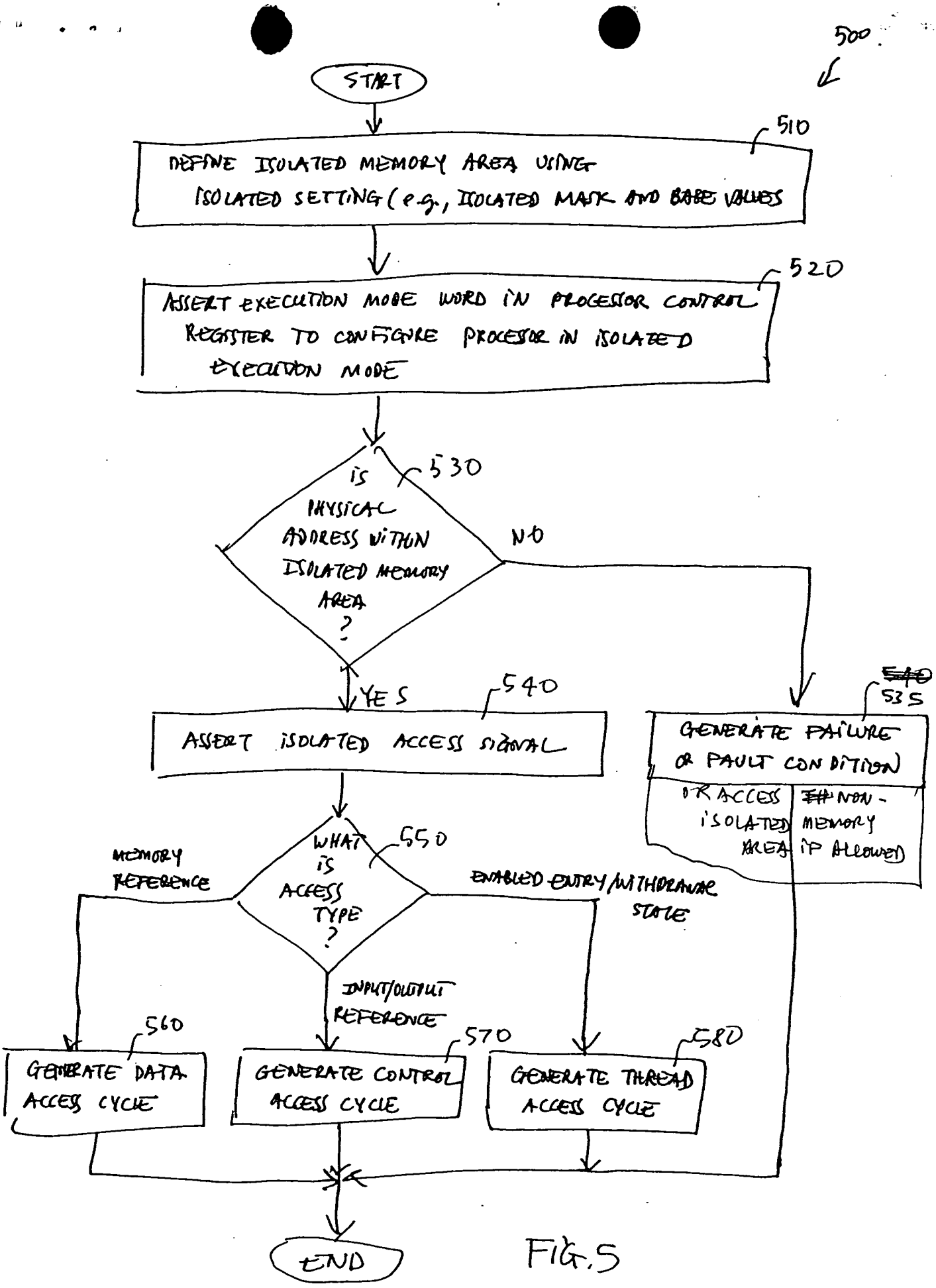

500
START
510
DEFINE ISOLATED MEMORY AREA USING ISOLATED SETTING (e.g., ISOLATED MASK AND BASE VALUES
520
ASSERT EXECUTION MODE WORD IN PROCESSOR CONTROL REGISTER TO CONFIGURE PROCESOR IN ISOLATED EXECUTION MODE
530
IS PHYSICAL ADDRESS WITHIN ISOLATED MEMORY AREA ?
NO
YES
540
ASSERT ISOLATED ACCESS SIGNAL
535
GENERATE FAILURE OR FAULT CONDITION
OR ACCESS ISOLATED MEMORY AREA IF NON-ALLOWED
550
WHAT IS ACCESS TYPE ?
MEMORY REFERENCE
INPUT/OUTPUT REFERENCE
ENABLED ENTRY/WITHDRAWAL STATE
560
GENERATE DATA ACCESS CYCLE
570
GENERATE CONTROL ACCESS CYCLE
580
GENERATE THREAD ACCESS CYCLE
END

FIG. 5